NR

Code No: B5702, B5508

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M.Tech II Semester Examinations, October/November 2011
DESIGN FOR TESTABILITY
(COMMON TO VLSI SYSTEM DESIGN, EMBEDDED SYSTEMS)

Time: 3hours **Max. Marks: 60**

Answer any five questions
All questions carry equal marks

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1.a) Define the following fault models using examples.
i) Cross – Pint Fault ii) Multiple stuck – at fault iii) Transition fault

b) What is Equivalence and dominance fault collapsing? Derive the equivalence collapsed fault set in the given circuit shown in figure 1. [6+6]

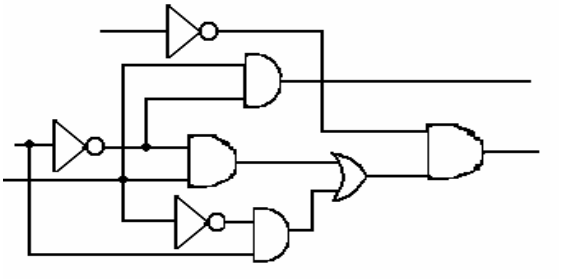

figure 1

2.a) Explain two different RTL Categories–Procedural and non procedural languages in describing the RTL model.

b) How are structural models represented? Draw the bipartite graph model for the circuit shown below in figure 2. [6+6]

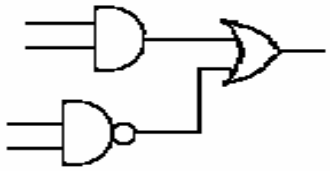

figure 2

3.a) Let N be a combinational circuit composed only of NAND gates. Assume that every primary input has only one fan out. Show that a test set that detects all SA1 faults in N detects all SA0 faults as well.

b) Prove that in a fan out free circuit, any pair of functionally equivalent faults are also structurally equivalent. [6+6]

4. Perform ATPG on the circuit shown in figure 3 using D- algorithm to test the fault in SA1. [12]

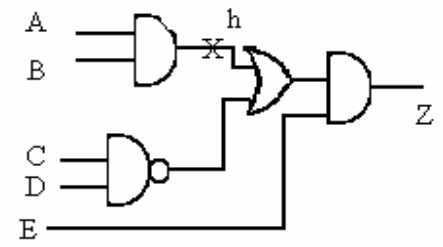

figure 3

Cont…2

5. Device a test for A SA1 fault in the circuit given in figure 4. Does the test provide a definite or a potential detection? [12]

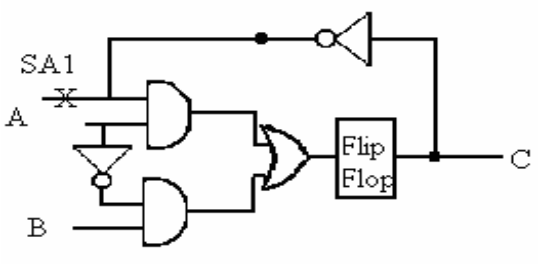

figure 4

6.a) How does controllability and observability improve with DFT.
b) Explain the Boundary Scan standards. [6+6]

7. Explain the tradeoff between ATEs and BIST. [12]

8. Write a brief note on
a) Signature analyzer
b) Embedded memory test model. [6+6]

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